



PATENT

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Nicolas Demange et al.  
Filed : July 15, 2003  
Application No. : 10/621,262  
For : METHOD OF FABRICATING A FERROELECTRIC  
STACKED MEMORY CELL

Docket No. : 854063.523C1  
Date : November 3, 2003

Mail Stop Missing Parts  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

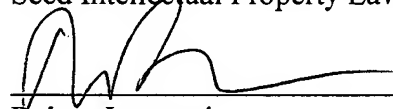
Commissioner for Patents:

In accordance with 37 C.F.R. §§ 1.56 and 1.97 through 1.98, applicants wish to make known to the Patent and Trademark Office the references set forth on the attached Form PTO-1449. This application is a Continuation in Part and relies, under 35 U.S.C. § 120, on the earlier filing date of prior Application No. 09/911,637, filed July 23, 2001, which is a divisional of prior Application No. 09/365,187, filed August 2, 1999, now US Patent No. 6,300,654. The references listed on the attached Form PTO-1449 were submitted to and/or cited by the Patent and Trademark Office in this prior application and, therefore, are not required to be provided in this application. If the Examiner wishes, copies will be provided upon request. As to any reference supplied, applicants do not admit that it is "prior art" under 35 U.S.C. §§ 102 or 103, and specifically reserve the right to traverse or antedate any such reference, as by a showing under 37 C.F.R. § 1.131 or other method. Although the aforesaid references are made known to the Patent and Trademark Office in compliance with applicants' duty to disclose all information they are aware of which is believed relevant to the examination of the above-identified application, applicants believe that their invention is patentable.

Please acknowledge receipt of this Information Disclosure Statement and kindly make the cited references of record in the above-identified application.

Applicants believe this Information Disclosure Statement has been timely filed, however, the Commissioner is authorized to charge any fee due by way of this Information Disclosure Statement to our Deposit Account No. 19-1090.

Respectfully submitted,  
Nicolas Demange et al.  
Seed Intellectual Property Law Group PLLC



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Enclosures:  
Form PTO-1449

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FORM PTO-1449  
(REV. 7-80)U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
854063.523C1APPLICATION NO.  
10/621,262

APPLICANTS

Nicolas Demange et al.

FILING DATE

July 15, 2003

GROUP ART UNIT

2812

INFORMATION DISCLOSURE STATEMENT  
(Use several sheets if necessary)

## U.S. PATENT DOCUMENTS

*EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
AA	5,350,705	09/27/94	Brassington et al.	257	295	
AB	5,418,388	05/23/95	Okudaira et al.	257	295	
AC	5,519,237	05/21/96	Itoh et al.	257	306	
AD	5,796,133	08/18/98	Kwon et al.	257	295	
AE	5,796,136	08/18/98	Shinkawata	365	306	
AF	5,955,758	09/21/99	Sandhu et al.	257	306	
AG	6,028,361	02/22/00	Ooishi	257	774	
AH	6,063,656	05/16/00	Clampitt	438	239	
AI						

## FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION	
				YES	NO
AJ					
AK					
AL					

## OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

AM	Amanuma, K. et al., "Capacitor-on-Metal/Via-stacked-Plug (CMVP) Memory Cell for 0.25um CMOS Embedded Fe RAM", <i>IEEE</i> , 1998, pg. 363-366.
AN	Jones, Robert E. Jr., "Integration of Ferroelectric Nonvolatile Memories," <i>Solid State Technology</i> , October 1997, pp. 201-210.
AO	Takashima, D. et al., "A Sub-40ns Random-Access Chain FRAM Architecture with a 7ns Cell-Plate-Line Drive," <i>IEEE International Solid-State Circuits Conference</i> , 1999, pp. 102-103.
AP	Yamazaki, T., et al., "Advanced 0.5um FRAM Device Technology with Full Compatibility of Half-Micron CMOS Logic device", <i>Advanced Process Integration Department, Fujitsu Limited. (4 pages)</i> .

EXAMINER

DATE CONSIDERED

\* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).